IEEE Open Journal of
Power Electronics

Received 21 October 2023; revised 19 November 2023; accepted 26 November 2023. Date of publication 12 December 2023; date of current version 22 February 2024. The review of this article was arranged by Associate Editor Lijun (GAE | OJ GE) Hang. This work was submitted for review to OJPEL Special Compendium on Digital Design of Power Electronics Device and Equipment on 21st Oct. 2023.

*Digital Object Identifier 10.1109/OJPEL.2023.3341701*

# Analysis and Optimization of the Loss Distribution for a Two Stage AC/DC Power Supply

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This work was supported by the German Federal Ministry for Economic Affairs and Climate Action under Grant 03EN2010A-G.

**ABSTRACT** This paper presents the analysis and optimization procedure of a two-stage bidirectional AC/DC power supply. The exemplary power supply consists of a silicon carbide based active front end and a dual active bridge DC/DC converter. It is designed to supply 600 V DC applications from universal low voltage AC grids with a power up to 6 kW. The paper includes the topology and design considerations, as well as an in-depth loss distribution analysis based on a validated loss model. The loss model is then utilized for an operation space optimization. A special focus is drawn to the loss model and the optimization: It is based on analytical equations optimized for a low calculation effort. This enables quick modeling of a large operation space. Those results can both be used to validate design considerations as well as to optimize operating parameters. The presented dynamic operating parameter optimization enables a loss reduction at full load by 14% and at half load by even 48%. By means of the optimization the operating area can be expanded, losses decreased, and thermal stress reduced.

**INDEX TERMS** AC-DC power conversion, DC-DC power conversion, DC power systems, modeling, optimization methods, power electronics.

## I. INTRODUCTION

Current developments in industry and society lead to the need for high power AC/DC power supplies in low voltage grids (e.g., charging stations, energy storages, DC-grids for industry, on board chargers for special vehicles [1], [2], [3], [4]). In addition, bidirectional supplies are favored for future applications to feed power back into the grid (e.g., braking energy, integration of renewables and batteries, vehicle to grid). Energy prices, thermal stress and cost for cooling effort drive the need for highly efficient power supplies with lowest heat dissipation under all operating conditions. Trends in vehicular applications (more electric road, railway, air) as well as stationary applications (cabinet space, machine size) increase the need for more volume-efficient supplies with higher power-densities [5], [6]. A wide input voltage range is required to support universal grid voltages [7].

This paper presents the optimization by operating parameter adaptation of a three phase, 6 kW power supply designed with high power density and high efficiency.

Recently, much work has been published on design space optimization [8], [9], [10], [11]. Design space optimization can help increase efficiency, power density, and reduce cost for a given operating point [11]. However, the results presented in this paper reveal an additional potential of optimizing operating parameters after the design is fixed. Especially in the context of a large operating space (e.g., wide input voltage ranges, adjustable output voltage, partial load operation), the use of an optimization algorithm to find suitable operating parameters (e.g., DC-link voltages, switching frequencies) reduces losses and thermal stress.

Current relevant work on loss models for wide bandgap (WBG) based power converters was, amongst others, published in [12], [13], [14], [15]. The introduced analytical

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**TABLE 1. Excerpt of International Grid Voltages [7]**

| Country / Region | Three Phase line to line grid voltage(s) |
|---|---|
| EU | 400 V |
| USA/Canada | 208 V, 480 V , 600 V |
| Japan | 200 V |
| China | 380 V |

loss model presents a trade-off between calculation speed, accuracy, and flexibility. Compared to the analytical approach in [12], fewer and simpler calculation steps are needed. By differentiating between three transition types, accuracy and usability at high ripple currents is improved compared to [14], [15]. Fastest models as in [13] rely on pre-calculated or measured look-up tables. To increase flexibility, the presented model is based on analytical equations. The magnetics loss model based on [16], [17] is simplified for the specific application in power electronic converters and possibilities for pre-calculation are exploited.

The design of the exemplary power supply (system specification, component, and topology selection) is based on references and is briefly presented in Ch. II and Ch. III. For optimizing design and operation, a detailed, precise yet calculation efficient modeling approach is developed and explained in detail in Ch. IV. The loss model is verified by comparison to measurement results of a built-up power supply (Ch. V and Ch. VI) and used to optimize its operating parameters for different operating conditions (Ch. VII and Ch. VIII).

## II. SYSTEM SPECIFICATION

The power supply is designed to supply loads up to 6 *kW* at a controlled DC output voltage of 600 V from universal three phase low voltage grids. Table 1 gives an overview of different international nominal grid voltages. For universal applicability at affordable cost the supply is specified to work in grids from nominal 200 V to 480 V line to line AC voltage. Support of grids with an AC-voltage of 600 V would have a large influence on component selection and design and would thus counteract a volume and efficiency optimized design.

The DC output voltage is set to $V_{\mathrm{DC}} = 600$ V with an adjustable range from 550 V to 700 V. The output voltage of 600 V results from the rectified operating voltage range of available off-the-shelf inverters ($V_{\mathrm{AC,ll}} =$ 380 V . . . 480 V, *comp.* [18].); the output voltage range enables to comply with different upcoming standards for future DC-grids [2], [4], [19], [20]. For system efficiency optimization the output voltage can be adjusted (lower voltage → lower switching losses, higher voltage → lower conduction losses).

As connections to open DC-grids as in [2], [4], [19], [20] are possible applications for the presented power supply, a galvanic isolation is favored, especially when the grids are supposed to have an independent earthing concept (e.g., grounded Δ-AC-grid to mid-point grounded DC-grid). Also, when connecting multiple supplies in parallel, an isolation can help reduce circular currents between the converters.

**TABLE 2. Specification of the AC/DC-Power Supply**

| Specified Value | Value |
|---|---|
| Input voltage range ($V_{\mathrm{AC,ll}}$) | 200 V ... 480 V |
| Output voltage ($V_{\mathrm{DC,Out}}$) | 600 V (550 V ... 700 V) |
| Power | 6 kW |
| Isolation type | Reinforced acc. [21] |

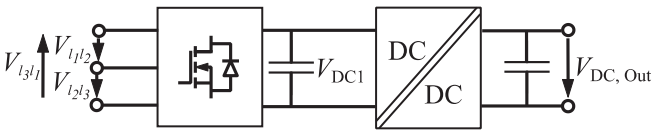


**FIGURE 1. Block diagram of a two stage AC/DC power supply with a three-phase input ($L_1$, $L_2$, $L_3$) and DC output ($V_{\mathrm{DC,Out}}$).**

**TABLE 3. Specification of Bidirectional Active Rectifier**

| Specified Value | Value |
|---|---|
| Input voltage range ($V_{\mathrm{AC,ll}}$) | 200 V…480 V |
| DC-link voltage range ($V_{\mathrm{DC1}}$) | 300 V…750 V |
| Power | 6 kW |
| Power flow | Bidirectional |

A resulting exemplary specification is given in Table 2. The findings presented in the following chapters may be adopted to any other multi-stage power-electronics based converter.

## III. SYSTEM SPECIFICATION AND DESIGN CONSIDERATIONS

A block diagram of the investigated system is given in Fig. 1. The system consists of two stages: A bidirectional active front end (AFE) and a bidirectional, galvanically isolated DC/DC converter.

### A. TOPOLOGY CONSIDERATIONS

Both, the AFE as well as the DC/DC converter must provide bidirectional power flow. Due to the recent developments in wide bandgap (WBG) technologies, efficient converters can be built with Silicon Carbide (SiC) MOSFETs in a standard two-level topology [22]

For the AFE, a three leg, two-level inverter with an integrated All-Pole-LC filter is used. Due to the use of high switching frequencies (∼100 kHz), it is possible to reduce the volume of the LC-filter components compared to conventional AFEs (2 . . . 16 kHz switching frequency) and integrate it in one housing with the AFE [23].

The specified values for the AFE are shown in Table 3: The input voltage range corresponds to the input voltage range of the complete power supply. The AFE output voltage is the DC-link voltage $V_{\mathrm{DC1}}$. To enable a system optimization, the AFE must support a large voltage range for the DC-link voltage and its range must comply with the maximum input

**TABLE 4. Specification of the DC/DC Converter**

| Specified Value | Value |
|---|---|
| Input voltage range ($V_{DC1}$) | 300 V ... 750 V |
| Output voltage ($V_{DC,Out}$) | 600 V (550 V ... 700 V) |
| Power | 6 kW |
| Power flow | Bidirectional |
| Isolation | Reinforced acc. [21] |

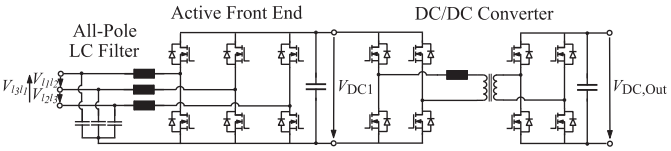


**FIGURE 2. Schematic diagram of a two stage AC/DC power supply with a three-phase input ($L_1$, $L_2$, $L_3$) and DC output ($V_{DC,Out}$).**

voltage $V_{AC,ll}$, while allowing a control reserve $R_{C,\%}$:

$$V_{DC1,\,min} = V_{AC,ll} \cdot \sqrt{2} \cdot \left(1 + R_{C,\%}\right) \tag{1}$$

Additionally, a 10% margin for voltage fluctuations [7], [24] should be considered. For the defined input voltage range this results in an operating DC-link voltage range of 300 V …750 V.

The losses of the AFE mainly depend on the DC-link voltage (switching and AC-filter losses) and input current (switching and conduction losses) [25]. The highest losses at a given power thus appear for a low input voltage (following high input currents) and a high DC-link voltage.

The specification of the DC/DC stage is shown in Table 4. It complies with the DC-link voltage range of the AFE as an input voltage and the power supply output voltage range as output voltage. Further, the DC/DC converter must provide the galvanic isolation.

Many different DC/DC converter topologies can be found in literature [26], [27], [28]. However, for resonant topologies in higher power applications (>2 kW), expensive capacitors are needed in addition to the transformer. Also, resonant topologies tend to have a limited bidirectional capability in terms of transfer ratio: In one direction, most resonant topologies have a maximum transfer-ratio equal to the transformer turns ratio. Thus, operated at a high AC input voltage $V_{AC,ll}$ and thus a high DC input voltage $V_{DC1}$ energy transfer to the grid may not be possible at $V_{DC,Out} < V_{DC1,min}$. To provide full bidirectionality, be able to vary the DC-link voltage and to lower component cost, a dual active bridge (DAB) is chosen for the DC/DC converter.

### B. SYSTEM DESCRIPTION

A resulting overview schematic is given in Fig. 2. All power semiconductors are assumed to be SiC MOSFETs, which allow a high switching frequency as well as a high efficiency for the given voltage levels [22]. All half bridges are 2-level configurations to keep the component count and cost low.

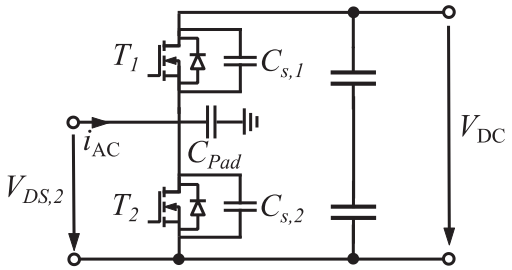


**FIGURE 3. Circuit diagram of a half bridge switching cell with parasitic capacitances.**

To comply with electromagnetic compatibility (EMC) standards, a grid filter in front of the AFE is needed [29]. The examined filter topology is an all-pole LC-filter, that damps common as well as differential mode currents.

The input and output stage of the DAB converter are comprised of full bridges to utilize the full voltage range at the input and output stage and thus reduce the currents. Also, this configuration enables the use of the third level and thus advanced modulation strategies [30], [31], [32].

## IV. MODEL DESCRIPTION

The presented loss model can be divided into component loss models and topology dependent current/voltage models. The components models include a half bridge semiconductor loss model as well as the magnetic loss models both for the LC-filter chokes and for the medium frequency transformer. The topology dependent current models are described for the AFE and the DC/DC converter separately and may be extended to further topologies.

### A. COMPONENT LOSS MODELS

#### 1) SEMICONDUCTOR LOSS MODELING

The semiconductor losses mainly depend on the RMS current, the current during the switching instance, the DC-link voltage as well as the component parameters and the drive circuit. They are mainly distinguished into switching and conduction losses while neglecting some additional smaller losses like leakage or driving losses.

*a) Switching losses:* While the component parameters are given by the semiconductor manufacturer, the switching currents are calculated. Most simple models assume hard switching for all transitions. Especially with WBG semiconductors higher ripple currents are possible and thus more soft transitions may occur and have a large influence on the switching losses. In Fig. 3, the schematic diagram of the half bridge switching cell with parasitic capacitances is shown. With double pulse tests, distinguishing between capacitor currents (currents into $C_s$) and channel currents (currents through $T$) is not possible (comp. [33]). While many models neglect this difference, the presented approach separates those currents and calculates the losses accordingly.

The total switching capacitance $C_{ac}$ is given by the sum of the output capacitances of the MOSFETs $C_{s,i}$ (charge related

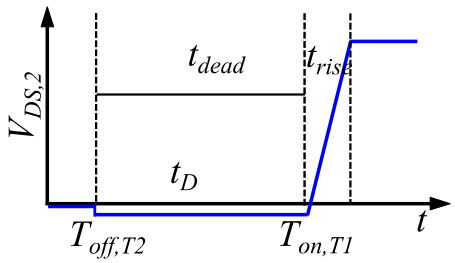


**FIGURE 4.** $V_{DS,2}(t)$ at hard transition ($i_{AC} < 0$).

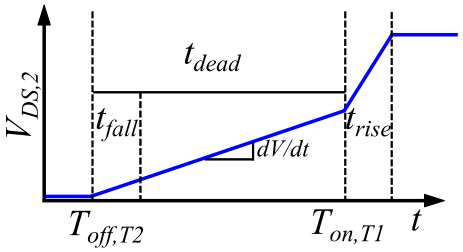


**FIGURE 5.** $V_{DS,2}(t)$ at mixed transition $0 < i_{AC} < \frac{C_{ac} \cdot V_{DC}}{t_{dead}}$.

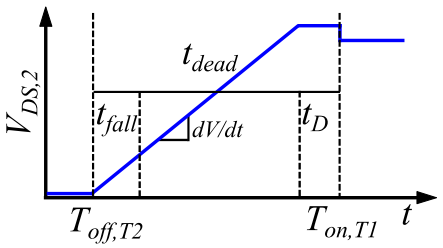


**FIGURE 6.** $V_{DS,2}(t)$ at soft transition ($i_{AC} > 0$).

capacitance) and the parasitic capacitance of the switching node $C_{Pad}$, while the parasitic capacitance of the inductor is neglected:

$$C_{ac} = C_{s,1} + C_{s,2} + C_{Pad} \tag{2}$$

One switching instance always describes the transition from one semiconductor in the on state to the other being turned on. As the switching processes are nearly the same for the transitions from $T_1$ conducting to $T_2$ conducting and vice versa, here only the transition from $T_2$ to $T_1$ is described in detail.

For each switching instance, three cases are distinguished:

I. Hard transition: $C_{ac}$ must be charged by the turned-on semiconductor.
II. Mixed transition: $C_{ac}$ is only partially charged during the dead time: $i_{AC} < \frac{C_{ac} \cdot V_{DC}}{t_{dead}}$
III. Soft transition: $C_{ac}$ is charged by the inductor current within the dead-time.

The voltage waveforms for all three transitions are shown in Figs. 4–6. Here $t_{rise}$ and $t_{fall}$ refer to the rise and fall time of the MOSFET respectively. The dead time is represented by $t_{dead}$, $t_D$ describes the diode conducting time.

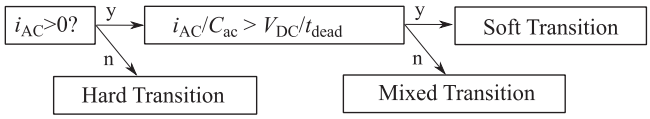


**FIGURE 7.** Switching loss calculation flowchart for transition from $T_2$ to $T_1$.

Fig. 7 shows the algorithm flowchart to decide which transition will occur for the transition from $T_2$ to $T_1$.

Losses can only occur, when the voltage and the current at the transistor are unequal to zero. However, it is important to distinguish between charging currents of the parasitic output capacitance and channel currents inside the MOSFET.

The losses are separated into turn-off losses $E_{off}$, turn-on losses $E_{on}$, diode losses $E_D$, charging losses $E_{chg}$, and reverse recovery losses $E_{rr}$. Turn-on, turn-off, and diode loss energies are calculated with the integral over the apparent power loss during the transition with the transistors drain source voltage $v_{DS}$ and the input current $i_{AC,i}$. The half bridge input current at a switching instance $i_{AC,i}$ is assumed to be constant during the switching instance:

$$E_{loss} = \int v_{DS} \cdot i_{AC,i} dt = i_{AC,i} \int v_{DS} dt \tag{3}$$

As the voltage waveform is approximated by a linear transition, the losses can be calculated with the turn-off and turn-on time $t_{fall}$ and $t_{rise}$, the total switching capacitance $C_{ac}$, the DC link voltage $V_{DC}$, the dead time $t_{dead}$, and the reverse-recovery charge $Q_{rr}$:

$$E_{off} = \frac{(i_{AC,i} \cdot t_{fall})^2}{2 \cdot C_{ac}} \tag{4}$$

$$E_{on} = \frac{V_{DC} \cdot i_{AC,i} \cdot t_{rise}}{2} \tag{5}$$

$$E_D = t_{dead} \cdot V_D \cdot i_{AC,i} \tag{6}$$

$$E_{rr} = \frac{1}{3} \cdot Q_{rr} \cdot V_{DC} \text{ [34]} \tag{7}$$

$$E_{chg} = \frac{(V_{DC})^2 \cdot C_{ac}}{2} \tag{8}$$

By calculating turn on / turn off losses ($E_{off}$, $E_{on}$) apart from the charging related losses $E_{chg}$, the model differentiates charging and channel currents for the different transitions. A deep discussion on the differentiation between channel and charging currents is given in [35]. The addition in dependence of the occurring transition leads to the switching energies:

$$E_{sw,i} = \begin{cases} E_{chg} + E_{on} + E_{rr} + E_D & (I) \\ E_{off} + \frac{1}{2}\left(V_{DC} - \frac{t_{dead} \cdot i_{AC,i}}{C_{ac}}\right)^2 \cdot C_{ac} & (II) \\ E_D + E_{off} & (III) \end{cases} \tag{9}$$

The average switching energy $\overline{E_{sw}}$ can be calculated with the $N$ transition points over one (fundamental or switching)

period (e.g., $N = 2$ for one switching period):

$$\overline{E_{\mathrm{sw}}} = \frac{1}{N} \cdot \sum_{i=1}^{N} E_{\mathrm{sw},i} \tag{10}$$

With the switching frequency $f_{\mathrm{s}}$, the switching power losses $P_{\mathrm{sw}}$ can be modeled:

$$P_{\mathrm{sw}} = \overline{E_{\mathrm{sw}}} \cdot f_{\mathrm{s}} \tag{11}$$

*b) Conduction losses:* The conduction losses are calculated with the currents Fourier components $a_{k,\mathrm{avg}}$ of the current and the on-state resistance of the MOSFET $R_{\mathrm{DS,on}}$ for the $M$ most relevant frequencies:

$$P_{\mathrm{cond}} = \sum_{k=0}^{M} R_{\mathrm{DS,on}} \cdot a_{k,\mathrm{avg}}^2 \tag{12}$$

### 2) MAGNETICS LOSS MODELING

Magnetic losses depend on many different parameters: Core material, winding configuration, used litz-wire, temperature and current [16]. However, calculation of such complex models for each optimization step is not useful and would not be an efficient solution. Since many of those parameters will not change during runtime, it is possible to simplify the model beforehand and use the simplified model for loss calculation.

*a) Winding losses:* Winding losses depend on the amplitude and the frequency of the current. It is possible to model those losses with a frequency dependent resistance $R(f)$ [16]. This resistance includes all winding losses including ohmic losses as well as skin and proximity effect. $R(f)$ can be found using FEMM simulations. The winding losses can then be calculated for $K$ windings with the $M$ most relevant frequencies and the currents Fourier components $a_{\mathrm{avg},i,j}$:

$$P_{\mathrm{loss,winding}} = \sum_{j=0}^{K} \sum_{i=0}^{M} R_j\,(f_i) \cdot a_{\mathrm{avg},i,j}^2 \tag{13}$$

With this approach, the tradeoff between accuracy and complexity can be easily adjusted by the number of evaluated frequencies $M$. The calculation during runtime is a convolution and thus very efficient.

*b) Core losses:* The core losses are calculated with the improved generalized Steinmetz equation (IGSE) [17]. The material parameters $\alpha$, $\beta$ and $k_{\mathrm{s}}$ are given or calculated in advance. As for high switching frequencies core materials such as powder or ferrite are used, core losses induced by low frequency components (e.g., 50 Hz, 60 Hz) can be neglected and only the ripple related core losses need to be calculated.

The integral of the IGSE (14) can be simplified to (15), where $m_{\mathrm{k}}$ is the core mass, $B$ the flux density and $\Delta B_{\mathrm{pp}}$ the peak-to-peak flux density difference:

$$P_{\mathrm{loss,core},i} = k_{\mathrm{s}} \cdot m_{\mathrm{k}} \cdot \frac{1}{2T} \int_{t}^{t+T} \left|\frac{dB}{dt}\right|^{\alpha} \left(\Delta B^{\beta-\alpha}\right) dt \text{ [6]} \tag{14}$$

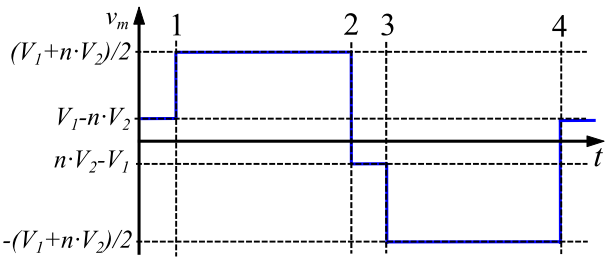


**FIGURE 8.** Typical voltage waveform of the voltage $v_m$ at the magnetizing inductance $L_m$ of a DAB transformer with indicated switching instances 1...4.

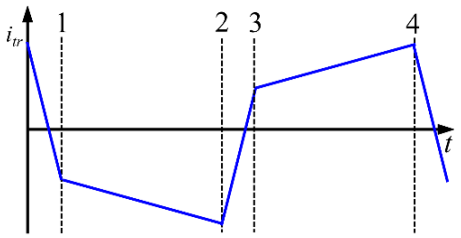


**FIGURE 9.** Typical transformer current waveform $i_{tr}$ of a DAB converter with indicated switching instances 1...4.

$$P_{\mathrm{loss,core},i} = 2 \cdot k_{\mathrm{s}} \cdot m_{\mathrm{k}} \cdot \left|\Delta B_{\mathrm{pp}}\right|^{\beta-\alpha} \cdot \left(\left(2 \cdot \frac{\Delta B_{\mathrm{pp}} \cdot f_{\mathrm{s}}}{1-\Phi_{\%}}\right)^{\alpha}\right) \tag{15}$$

## B. TOPOLOGY SPECIFIC PARAMETER MODEL

The topology specific parameter models must provide currents and voltages to calculate the device losses with the according equations.

### 1) DC/DC CONVERTER PARAMETER MODEL

The power transfer of the dual active bridge depends on the phase shift between primary and secondary switching bridge. For single phase shift modulation, the phase shift $\phi$ can be expressed in dependence of the transferred power $P$, the input and output voltage $V_1$ and $V_2$ and the transformers stray inductance $L_\sigma$ and turns ratio $n$:

$$\Phi_{\%} = \frac{\mathrm{sgn}\,(P)}{2} \cdot \left(\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2 \cdot \mathrm{abs}\,(P) \cdot f_{\mathrm{s}} \cdot L_\sigma}{n \cdot V_1 \cdot V_2}}\right) \tag{16}$$

*a) Current modeling:* The current modeling must provide currents for both the semiconductor loss model as well as the magnetics loss model. The semiconductor loss model needs currents at commutation instances to calculate switching losses. RMS currents are needed to calculate the semiconductor conduction losses. The magnetics loss model needs the Fourier coefficients of the current to calculate winding losses and the voltage waveform to calculate core losses.

(1) Currents at Commutation

The commutation points for the primary and secondary switching bridge are shown in Figs. 8 and 9 in respect to

the voltage at the magnetizing inductance (Fig. 8) and the transformer current (Fig. 9).

In forward operation points 1 and 3 are the commutation of the secondary bridge; points 2 and 4 of the primary bridge. All calculations are done for the primary side and transformed for the secondary by means of the transformer turns ratio. Equations (17) and (18) provide the currents for the primary half bridge at switching instances 1 through 4. $T_s = 1/f_s$ is the switching period, and $\Delta T = \Phi_\% \cdot T_s$ is the time shift between primary and secondary full bridge, where $\Phi_\%$ is the percental phase shift.

$$i_{1,3} = \pm\frac{\Delta T}{2} \cdot \frac{V_1 + n \cdot V_2}{L_s} - \frac{T - |\Delta T|}{4} \cdot \frac{V_1 - nV_2}{L_s} \tag{17}$$

$$i_{2,4} = \mp\frac{\Delta T}{2} \cdot \frac{V_1 + n \cdot V_2}{L_s} + \frac{T - |\Delta T|}{4} \cdot \frac{V_1 - nV_2}{L_s} \tag{18}$$

(a) Fourier analysis of DAB current

To simplify the analytic Fourier analysis of the DAB current, the first half of the current waveform is mirrored leaving only positive frequency components in the Fourier spectrum. The Fourier coefficients $a_k$ can be expressed by means of the commutation times $t_{1\ldots4}$, the currents at commutation $i_{1\ldots4}$ and the switching period $T_s = 1/f_s$:

$$\begin{aligned} a_k \cdot \frac{T_s}{4} &= \int_0^{t_1} \frac{i_1}{t_1} \cdot t \cdot \sin(2\pi \cdot k f_s t)\, dt \\ &+ \int_{t_1}^{t_2} \left( \frac{i_2 - i_1}{t_2 - t_1} \cdot (t - t_1) + i_1 \right) \cdot \sin(2\pi \cdot k f_s t)\ dt \\ &+ \int_{t_2}^{T_s/2} \left( -\frac{i_1}{t_1} \cdot (t - t_2) + i_2 \right) \cdot \sin(2\pi \cdot k f_s t)\ dt \end{aligned} \tag{19}$$

*b) Medium frequency transformer flux density modeling:* The flux density can be calculated with the voltage $v_m$ at the magnetizing inductance $L_m$ as well as the core cross section $A_k$ and the primary number of turns $N_1$. The voltage waveform $v_m$ is shown in Fig. 8. If $V_1 - n \cdot V_2 \ll \frac{1}{2} \cdot (V_1 + n \cdot V_2)$, the peak-to-peak flux density $\Delta B_{pp}$ can be approximated with the percental phase shift $\Phi_\%$, the input and output voltage $V_1$ and $V_2$, the transformer turns ratio $n$, core cross section $A_k$ and primary turns number $N_1$ and the switching frequency $f_s$:

$$\Delta B_{pp} = (1 - \Phi_\%) \cdot \frac{(V_1 + n \cdot V_2)/2}{2 \cdot A_k \cdot f_s \cdot N_1} \tag{20}$$

### 2) ACTIVE RECTIFIER PARAMETER MODEL

*a) Current and duty ratio modeling:* The phase currents including the ripple current must be modeled. For this purpose, the RMS input current as well as the input voltage and the DC-link voltage are needed. The model is given for a neutral point connected LC-filter as shown in Fig. 10. All three phases are independent and thus all calculations are only shown for one half bridge.

(1) Duty Ratio

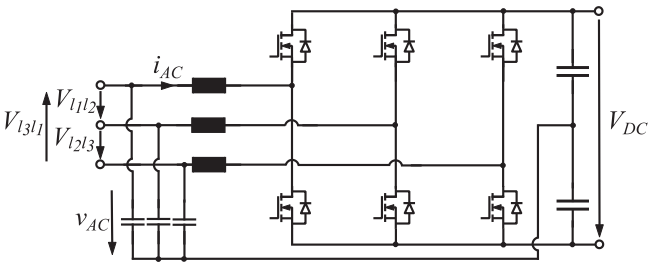


**FIGURE 10.** Circuit diagram of the investigated inverter system.

The duty ratio $d$ is important for modeling the current. Modern inverter systems are often operated in overmodulation. Thus, it is important to consider not only sinusoidal modulation but also different overmodulation strategies [36].

*(a) Sinusoidal Modulation*

The duty ratio $d$ for sinusoidal modulation can be calculated with the phase voltage $v_{AC}$ and the DC-link voltage $V_{DC}$:

$$d(t) = \frac{v_{AC}(t)}{V_{DC}} + \frac{1}{2} \tag{21}$$

*(b) Overmodulation*

To realise a modulation index M>1, overmodulation is used [36], which must be considered in the loss model. As many different overmodulation strategies exist in literature (cf. [36]) and even more proprietary strategies are implemented, the loss model is adapted to allow arbitrary modulation forms. It is set by replacing the calculation of the duty ratio by an arbitrary function:

$$d(t) = f(v_{AC}(t)) \tag{22}$$

*b) Fundamental current and voltage:* The fundamental current component is controlled and for the exemplary case will be assumed to be sinusoidal and in phase with the grid voltage $v_{AC}$. Then, $v_{AC}(t)$ can be expressed with the RMS input voltage $V_{AC,rms}$ and the input (grid) frequency $f_G$:

$$v_{AC}(t) = \sqrt{2} \cdot V_{AC,rms} \cdot \sin(2\pi \cdot f_G \cdot t) \tag{23}$$

Using the model for high switching frequencies, the phase difference between grid and modulated voltage can be neglected. The current can be expressed with the RMS input current $I_{rms}$ and the input (grid) frequency $f_G$:

$$i_{AC}(t) = \sqrt{2} \cdot I_{rms} \cdot \sin(2\pi \cdot f_G \cdot t)\,. \tag{24}$$

*c) Ripple current:* The filter resonance frequency $f_r$ must be designed much lower than the switching frequency $f_s$ of the converter [29]. Thus, the capacitor voltage $V_C$ can be assumed as constant over one switching period. The peak-to-peak ripple current $\Delta I_{pp,i}$ for a given input voltage $V_{AC,i} = v_{AC}(t_i)$ and given DC-link voltage $V_{DC}$ can be calculated with the inductance of the LC-filter inductor $L$:

$$\Delta I_{pp,i} = \frac{(V_{DC}/2 - V_{AC,i}) \cdot (V_{AC,i} + V_{DC}/2)}{f_s \cdot L \cdot V_{DC}} \tag{25}$$

With the assumption of an asymmetric triangular current waveform the Fourier coefficients $a_{k,i}$ of the ripple current can be calculated efficiently with the duty ratio $d_i = d(t_i)$ [25]:

$$\frac{a_{k,i}}{\Delta I_{\mathrm{pp},i}} = \frac{2\left(\sin\left(\pi d_i k\right) - \sin\left(\pi k\right) + \pi\left(1-d_i\right)\cdot\cos\left(\pi d_i k_i\right)\right)}{\pi^2\cdot\left(1-d_i\right)\cdot k^2} + \frac{2\sin(\pi d_i k) - 2\pi d_i k\cdot\cos\left(\pi d_i k\right)}{\pi^2\cdot d_i\cdot k^2} \tag{26}$$

The average harmonic contents of the ripple current over one period is estimated by taking $N$ evenly distributed samples at the times $t_i$:

$$a_{k,\mathrm{avg}} = \sum_{i=0}^{N} a_{k,i} \tag{27}$$

#### 3) COMBINED CURRENT

The combined current at the switching instance $i$ results from the addition of both the ripple current component $\Delta I_{\mathrm{pp},i}$ and the fundamental current component $I_{\mathrm{AC},i} = i_{\mathrm{AC}}(t_i)$. For the switching losses, especially the currents at the switching instance are relevant. During the switching process, the current is assumed to stay constant. The currents for the transitions from low to high $I_{\mathrm{T2}\to\mathrm{T1}}$ and from high to low $I_{\mathrm{T1}\to\mathrm{T2}}$ can then be calculated:

$$I_{\mathrm{T2}\to\mathrm{T1}} = I_{\mathrm{AC},i} - \frac{\Delta I_{\mathrm{pp},i}}{2} \tag{28}$$

$$I_{\mathrm{T1}\to\mathrm{T2}} = I_{\mathrm{AC},i} + \frac{\Delta I_{\mathrm{pp},i}}{2} \tag{29}$$

For the inductor losses the Fourier coefficients are needed. As the fundamental current and the ripple current are at different frequencies, the Fourier coefficients can be seen as independent and the current results from the combination of all Fourier coefficients. The influence of the phase of the ripple current relative to the fundamental current can be neglected if different bias magnetization does not affect the losses.

### C. LOSS CALCULATION

The presented equations for the device loss calculation (semiconductors/magnetics) can now be combined with the topology specific parameter model to calculate the losses of each component. The results are presented in Ch. VII.

## V. MEASUREMENT RESULTS AND MODEL VERIFICATION

To verify the model, the power supply described in Ch. III was built up. For high efficiency and high power-density the power supply was built up using SiC-MOSFETs and an initial switching frequency of 100 kHz was chosen. However, the later presented modeling results reveal different optima regarding the switching frequencies for both AFE and DAB.

**TABLE 5. Relevant Components and Settings in Hardware Setup**

| | | |
|---|---|---|
| Semiconductors | Infineon IMZ120R090M1H | |
| DC Capacitors | Vishay MKP1848C, 900 V 50 µF | |
| AFE Inductor | Core Material | Sendust 60µ |
| | Core Size | 62x33x25 |
| | Turns | 35 |
| MF-Transformer | Core Material | Epcos N87 |
| | Prim. Turns | 12 |
| | Sec. Turns | 12 |
| | Litz Wire | 1400x0.05mm |
| Driving Voltage | On: 15 V | Off: 0 V |
| Switching Frequency | 100 kHz | |
| Dead Time | 160 ns | |

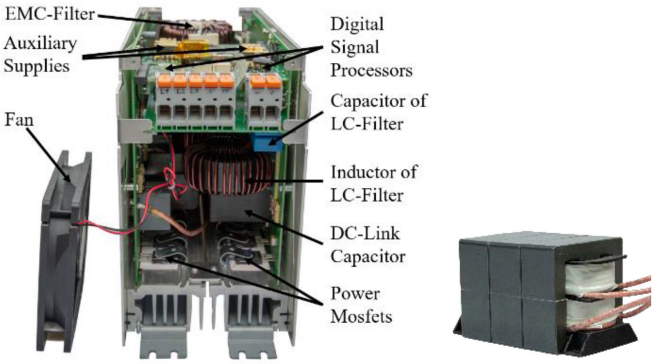


**FIGURE 11. Built-up power supply without housing and removed fan (left) and MF-transformer (right), which is located inside the housing behind the inductors.**

The transformer turns ratio is set to 1:1 for first evaluation. However, depending on preferred grids and operation conditions other optima may be found [37].

### A. HARDWARE DESCRIPTION

The hardware topologies are chosen as described in Ch. III. Table 5 shows the devices and materials used for the AFE and DC/DC converter.

The built-up power supply is shown in Fig. 11. The all-pole LC-filter, an additional EMI filter, auxiliary supply and the MF-transformer are integrated in the housing. It provides an overall power density of 0.6 kW/l.

### B. MEASUREMENT RESULTS AND MODEL VERIFICATION

For the model verification the losses of the AFE and the DC/DC converter are measured individually and compared to the modeling results.

All measurements were taken with the measurement equipment denoted in Table 6.

**TABLE 6. Measurement Equipment**

| Equipment | Type |
|---|---|
| Oscilloscope | Tek MSO Series 4, 500 MHz, 12 bit |
| Current Probe | TCP0030A |
| Voltage Probe | THDP0200 |
| Power Analyzer | Yokogawa WT1800 |

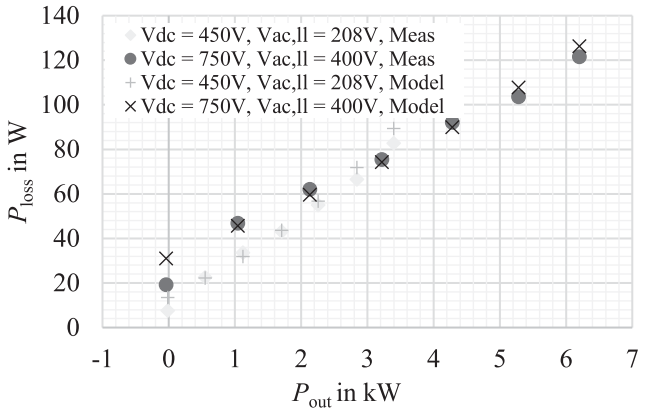


**FIGURE 12. Measured and modeled AFE losses at different powers $P_{Out}$ and different DC-link voltages $V_{DC1}$ at an input voltage of $V_{AC,ll}$ = 400 V and $V_{AC,ll}$ = 208 V.**

### 1) AFE MODEL VERIFICATION

The model is verified by comparison to the measurement results. In Fig. 12 a comparison between the simulated and measured losses is shown for two different operating points: Grey indicates the measurements and simulations at a DC-link voltage of 450 V and an RMS AC voltage of 208 V. Black indicates the measurements and simulations at a DC-link voltage of 750 V and an RMS AC voltage of 400 V. For both operating points the x-marker represents the model results while the bullet-marker represents the measurement results. In all points except open load the model can predict the losses very accurately. At open-load operation the deviation is 60% or 10 W. This reveals a poor estimation of constant losses by the model. However, for the optimization constant losses may be negligible. For $V_{AC,ll}$ = 400 V the relative deviation is smallest for medium power, for $V_{AC,ll}$ = 208 V the deviation increases with power. This indicates that current related losses ($E_{off}$, $E_{on}$, $E_D$) are slightly over-estimated while voltage related losses ($E_{chg}$, $E_{rr}$) are underestimated. When excluding the open load operation, the model's average deviation is at 3.5% (including the open load operation expands the average deviation to 12%).

### 2) DC/DC CONVERTER MODEL VERIFICATION

To validate the loss model of the DC/DC converter, measurements at different operating points are presented and compared to the model result.

Fig. 13 shows the results of modeling and measuring at different powers and input voltages. The average deviation over all measurements taken is 11.2% and provides a good basis for loss optimization of the overall power supply. Largest deviations can be found at the boundary between hard- and soft-switching operation. When applying the model for optimization, the optimum found should be verified for sensitivity to device tolerances.

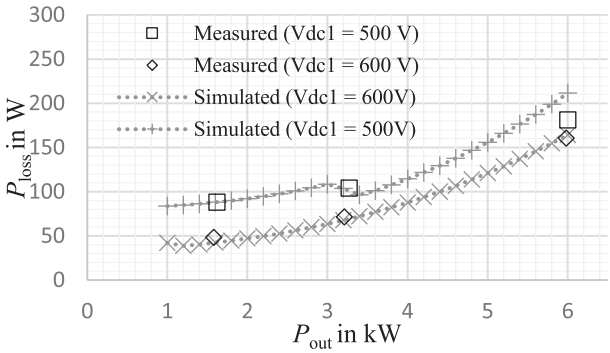


**FIGURE 13. Measured and modeled DAB losses at different powers $P_{Out}$ and different DC-link voltages $V_{DC1}$ at an output voltage of $V_{DC,Out}$ = 600 V.**

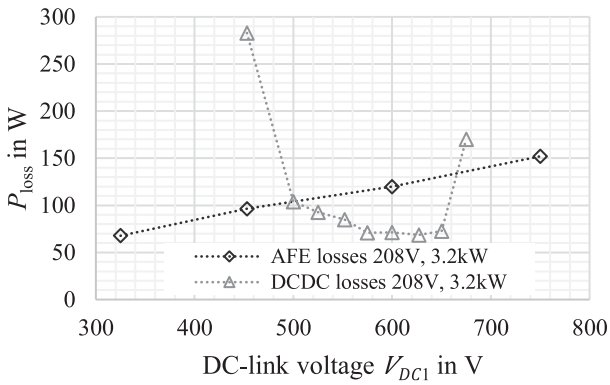


**FIGURE 14. Measured and interpolated losses at $P_{out}$ = 3.2 kW, $V_{AC,ll}$ = 208 V and $V_{DC,Out}$ = 600 V of the AFE and the DC/DC converter.**

## VI. SYSTEM MEASUREMENT RESULTS

### A. LOSS DISTRIBUTION

First, the losses of the AFE and the DC/DC converter are analyzed independently. Thermal monitoring of the AFE semiconductors temperature by thermocouple measurements during the loss measurements presented in Fig. 14 showed that with initial operating parameters the output power limit at $V_{AC,ll}$ = 208 V is $P_{out}$ = 3.2 kW. Thus, measurements with nominal power are only shown for $V_{AC,ll}$ = 400 V.

Fig. 14 shows the loss distribution among DC/DC converter and AFE at $P_{out}$ = 3.2 kW and $V_{AC,ll}$ = 208 V for different DC-link voltages $V_{DC1}$. Clearly, the loss distribution is influenced by the DC-link voltage: The AFE-losses increase nearly linearly with a higher DC-link voltage. The DC/DC converter losses increase strongly at transfer ratios far away from 1 (above 1.2 and below 0.9). Modeling results reveal that the converter leaves the soft switching region here. Between a DC-link voltage of $V_{DC1}$ = 500 V and $V_{DC1}$ = 650 V,

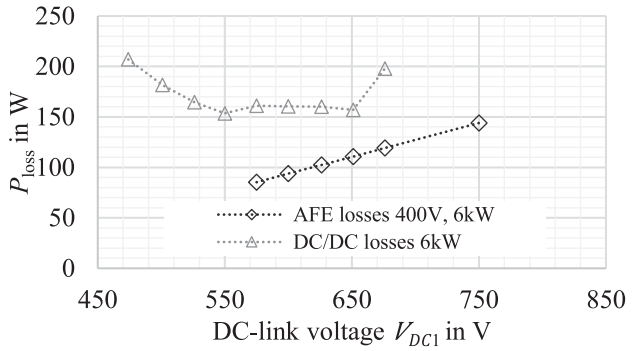


**FIGURE 15.** AFE and DC/DC converter losses at $P_{out} = 6$ kW, $V_{AC,ll} = 400$ V and $V_{DC,Out} = 600$ V in dependence of the DC-link voltage $V_{DC1}$.

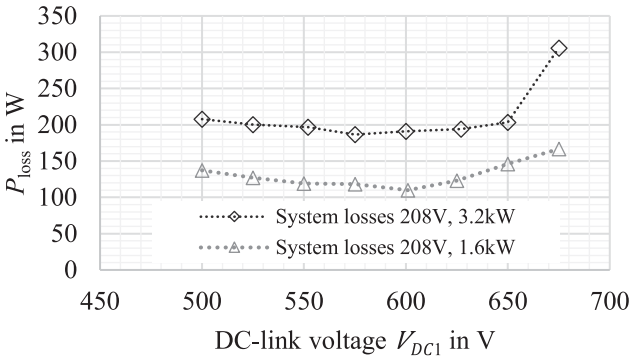


**FIGURE 16.** System losses at $V_{AC,ll} = 208$ V, $V_{DC,Out} = 600$ V in dependence of the DC-link voltage $V_{DC1}$ for different output powers.

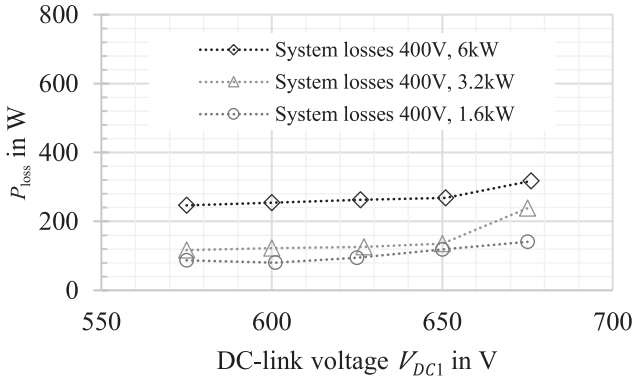


**FIGURE 17.** System losses at $V_{AC,ll} = 400$ V, $V_{DC,Out} = 600$ V in dependence of the DC-link voltage $V_{DC1}$ for different output powers.

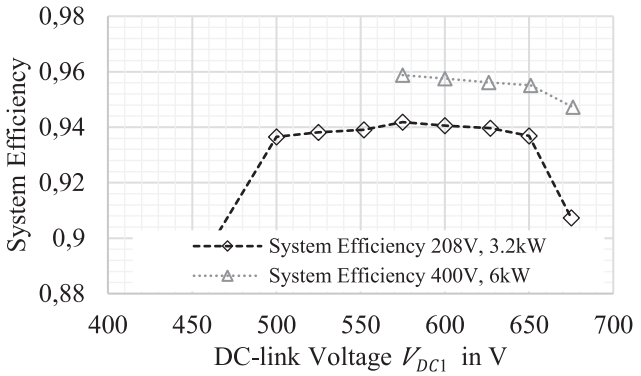


**FIGURE 18.** System efficiency for $P_{Out} = 3.2$ kW and $P_{Out} = 6$ kW in dependence of the DC-link voltage at input voltages of $V_{AC,ll} = 208$ V and $V_{AC,ll} = 400$ V, respectively, and an output voltage $V_{DC,\ out} = 600$ V.

the DC/DC converter losses slightly decrease with a rising DC-link voltage. In this region, the losses can be distributed among DC/DC converter and AFE by means of the DC-link voltage $V_{DC1}$. Minimum losses for the AFE can be found at $V_{DC1} = 500$ V; minimum losses for the DC/DC converter at $V_{DC1} = 625$ V. Further, for 500 V $\leq V_{DC1} \leq$ 650 V, the AFE losses dominate due to the low input voltage $V_{AC,ll}$.

Fig. 15 shows the losses of the DC/DC converter and AFE at $P_{out} = 6$ kW and $V_{AC,ll} = 400$ V in dependence of the DC-link voltage. The soft switching region is increased compared to the measurements at $P_{out} = 3.2$ kW. Minimum losses are at $V_{DC1} = 550$ V for the DC/DC converter and at $V_{DC1} = 575$ V for the AFE, respectively. It may be noted, that the AFE and thus the system must operate at $V_{DC1,\ min} \geq 575$ V for input voltages $V_{AC,ll} \geq 400$ V (cmp. (1)).

Figs. 16 and 17 show the overall losses for different power and input voltage levels. Fig. 16 includes the system losses at $V_{AC,ll} = 208\ V$, Fig. 17 at $V_{AC,ll} = 400\ V$.

At $V_{AC,ll} = 208$ V the lowest overall losses for 1.6 kW and 3.2 kW are at $V_{DC1} = 575$ V and $V_{DC1} = 600$ V respectively. However, losses of the AFE can be reduced by approximately 15% if operated at $V_{DC1} = 500$ V instead. This may be favorable as the AFE losses dominate for low input voltages.

Fig. 17 presents the system losses at $V_{AC,ll} = 400$ V at different output powers. At $P_{out} = 6$ kW and $P_{out} = 3.2$ kW, the system losses are minimum at $V_{DC1} = V_{DC1,min} = 575$ V. At $P_{out} = 1.6$ kW, losses become minimal at $V_{DC1} = 600$ V.

At all presented operating points, the DC/DC converter losses would yet be lower for higher DC-link voltages (cmp. Figs. 14 and 15). It may be concluded that for the presented operating points a transformer turns ratio smaller than 1:1 would be favorable in terms of system efficiency.

### B. SYSTEM EFFICIENCY

To complete the picture of the evaluated power supply, the overall system efficiency in dependence of the DC-link voltage $V_{DC1}$ is analyzed. The measurement results are given in Fig. 18.

Maximum efficiency for both $V_{AC,ll} = 400\ V$ as well as $V_{AC,ll} = 208$ V is achieved for a DC-link voltage of $V_{DC1} = 575$ V. Towards high/low transfer ratios between DC-link and output voltage, the efficiency drops clearly as the DAB leaves the soft switching region.

As the AFE-efficiency is much higher at larger input voltages $V_{AC,ll}$, the overall efficiency is higher at an input voltage of $V_{AC,ll} = 400$ V.

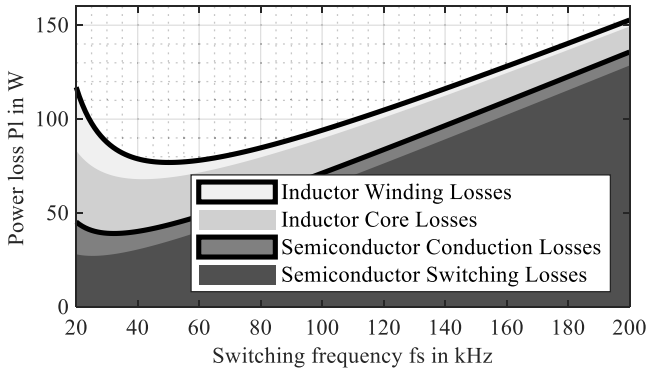


**FIGURE 19.** AFE losses in dependence of $f_{S,AFE}$ at a power of 5 kW, an input voltage of $V_{AC,ll} = 400$ V and a DC-link voltage of $V_{DC1} = 600$ V.

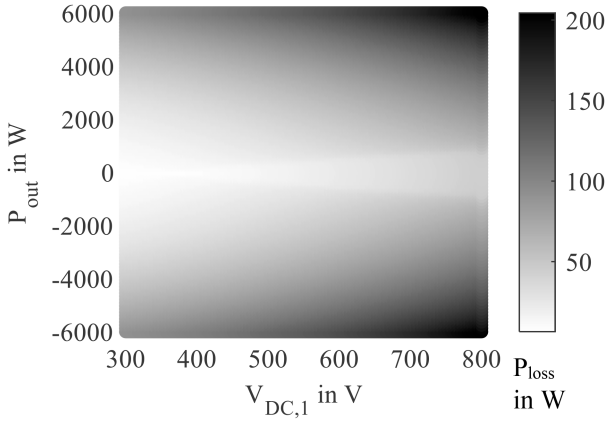


**FIGURE 20.** AFE model results for a parameter variation of $V_{DC,1}$ at $V_{AC,ll} = 208$ V.

## VII. MODEL RESULTS AND OPTIMIZATION

With the developed model, the systems losses can be modeled for arbitrary operating points and the loss distribution can be described. First, individual model and optimization results of the two stages are presented, secondly the optimization results for the complete power supply given.

### A. MODEL RESULTS OF THE AFE

#### 1) LOSS DISTRIBUTION AMONG COMPONENTS AND LOSS MECHANISM

Fig. 19 shows the AFE losses in dependence of the AFE switching frequency $f_{S,AFE}$. The optimum in terms of the overall losses is at $f_{S,AFE} = 52$ kHz. However, losses may be distributed between semiconductors and inductors: Minimum semiconductor losses are at $f_{S,AFE} = 34$ kHz.

#### 2) PARAMETRIC SIMULATION OF AFE LOSSES

To analyze the losses in the operation space, parametric simulations are conducted. Fig. 20 shows the results of the parametric simulation of the AFE losses for an input voltage of $V_{AC,ll} = 208$ V at a variable DC-link voltage $V_{DC1}$ and transfer power $P_{out}$. It is clearly visible, that the losses increase both with higher powers and with higher DC-link voltages. Further, around open load, the quasi-resonant region with lower losses can be seen.

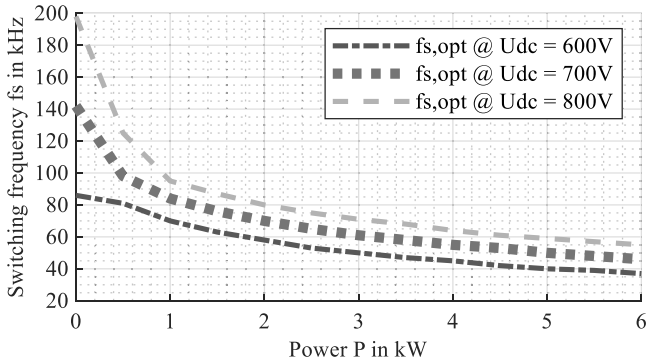


**FIGURE 21.** Diagram with the optimum AFE switching frequency $f_{S,AFE}$ for minimum AFE losses at different DC-link voltages $V_{DC1}$ in dependence of the power $P_{out}$ for an input voltage of $V_{AC,ll} = 400$ V.

#### 3) OPERATION SPACE OPTIMIZATION OF AFE

From the modeling and measurement results it is clear, that both the switching frequency as well as the DC-link voltage have a major influence on the AFE losses.

In terms of the AFE losses, the DC-link voltage should always be at its minimum (cmp. 5.3.2). However, in combination with the DC/DC converter, the DC-link voltage $V_{DC1}$ may be considered in the context of a system optimization.

The optimum switching frequency $f_{S,AFE}$ in dependence of the output power $P_{out}$ and the DC-link voltage $V_{DC1}$ can be found with an optimization algorithm. The allowable operating space for the AFE switching frequency is influenced by the filter's resonance frequency and the maximum frequency which dead-time, controller, and drive circuits can provide. Fig. 21 shows the result of a brute force optimization of the AFE switching frequency $f_{S,AFE}$ in dependence of the output power $P_{out}$ for different DC-link voltages $V_{DC1}$.

The optimum switching frequency $f_{S,AFE}$ is both dependent on the DC-link voltage $V_{DC1}$ as well as the transferred power: The higher the power, the lower the optimum switching frequency; the higher the DC-link voltage, the higher the optimum switching frequency. The reasons can be analyzed as follows: At lighter loads, the core losses dominate. As the inductance stays the same, $\Delta B_{pp,\,i}$ and thus the core losses decrease with a higher switching frequency (cmp. (14)). $\Delta B_{pp,\,i}$ and with it the influence of the core losses increases with higher DC-link voltages. Thus, the optimum switching frequency increases with higher DC-link voltages.

### B. MODEL RESULTS OF THE DC/DC CONVERTER

#### 1) LOSS DISTRIBUTION AMONG COMPONENTS AND LOSS MECHANISM

To analyze the distribution of the losses among the different components and loss mechanisms, Fig. 22 shows the losses in the DAB in dependence of the switching frequency $f_{S,DAB}$.

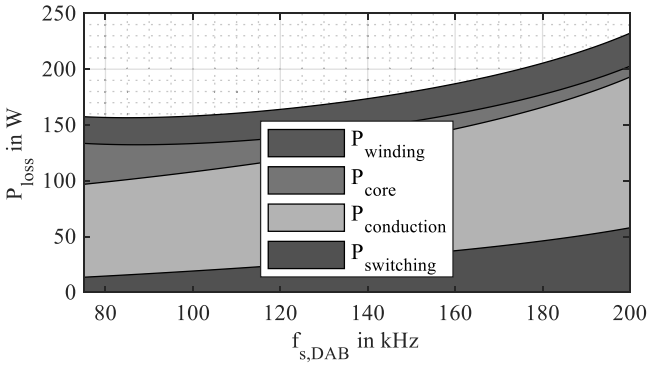


**FIGURE 22.** DAB loss distribution in dependence of switching frequency $f_{S,DAB}$ at a power of $P_{out} = 6$ kW.

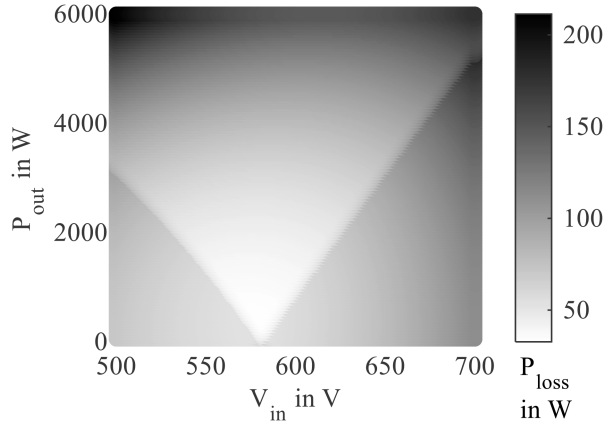


**FIGURE 23.** DAB model results for a parameter variation of $V_{DC1}$ at $V_{DC,\,out} = 600$ V.

The optimum switching frequency for a power transfer of 6 kW is at $f_{S,DAB} = 82$ kHz. However, between 75 kHz and 100 kHz, overall losses only slightly change. Thus, the loss distribution among the components may be optimized according to the model results: With higher switching frequencies, the losses can be moved from the magnetics towards the semiconductors.

### 2) PARAMETRIC SIMULATION OF DAB LOSSES

To get an overview of the losses in the operation space, a parametric loss simulation is shown in Fig. 23. Clearly visible is the soft switching area, that gets wider towards higher powers. Further, the influence of the magnetizing inductance can be seen: The soft switching region is slightly shifted towards the boost operation. At higher powers, where the ohmic losses clearly dominate inside the soft switching region, slight buck operation leads to the lowest power loss.

### 3) OPERATION SPACE OPTIMIZATION OF DAB

The DAB model shows that the minimal losses for a constant output voltage $V_{DC,Out}$ depend on the transferred power and the input voltage $V_{DC1}$.

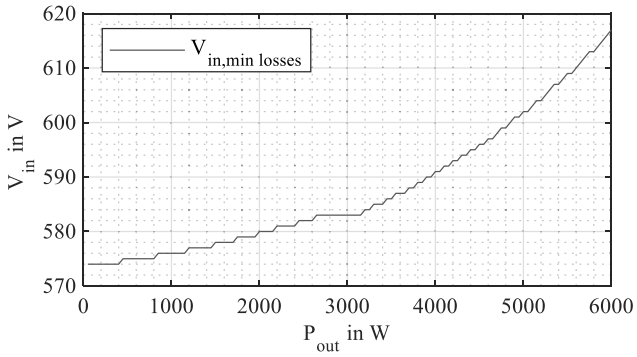


**FIGURE 24.** Optimum DAB input voltage $V_{DC1}$ in dependence of the transferred power at an output voltage of $V_{DC,\,out} = 600$ V and a fixed switching frequency of $f_{S,DAB} = 100$ kHz.

Fig. 24 shows the optimum input voltage $V_{DC1}$ in dependence of the transferred power. It can be seen, that with higher powers the optimum input voltage rises. In turn, to optimize the overall system losses, the DC-link voltage $V_{DC1}$ must be considered.

For the optimization of the switching frequency $f_{S,DAB}$, first the allowable operating space must be defined. To prevent saturation in the DAB transformer, the maximum volt-seconds must be considered.

In the presented design, the transformer is rated for an input and output voltage of 800 V at a switching frequency of 100 kHz. The maximum volt-seconds $A_{VT}$ can be calculated with the maximum input and output voltage $V_{DC,1}$ and $V_{DC,Out}$, the DAB switching frequency $f_{S,DAB}$ and the transformer turns ratio $n$:

$$A_{VT,max} = \frac{V_{DC,1,max} + V_{DC,Out,max}\ /n}{4 \cdot f_{S,DAB}} \tag{30}$$

The maximum switching frequency is limited by the digital controller and firmware architecture and the maximum allowable frequency in terms of power transfer. Thus, the limits for the DAB switching frequency can be defined with (30), the stray inductance $L_\sigma$, the output power $P_{out}$ and the transformer turns ratio $n$:

$$\frac{V_{DC1} \cdot V_{DC,Out}/n}{8 \cdot L_\sigma \cdot P_{out}} \geq f_{S,DAB} \geq \frac{V_{DC1} + V_{DC,Out}}{4 \cdot A_{VT,max}} \tag{31}$$

For this optimization, the switching frequencies upper limit is set to 200 kHz.

The optimization results are shown in Fig. 25. At lower powers two local optima can be found: at high switching frequencies as they reduce the transformer core losses and at medium frequencies due to the reduced switching losses. As an upper frequency limit exists there is a jump from the local optimum at medium frequencies to the maximum frequency for input voltages of $V_{DC,1} = 500$ V and $V_{DC,1} = 600$ V. At higher transfer powers the power independent core losses as well as the losses induced by the magnetizing current become less dominant. Instead, switching, winding and conduction losses are dominant. As winding and switching losses increase

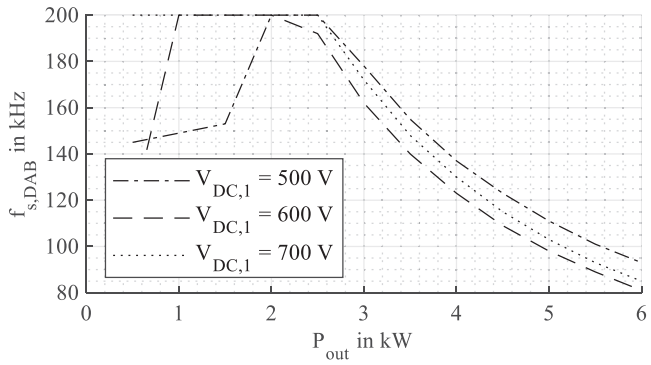


**FIGURE 25.** Optimum DAB switching frequency $f_{S,DAB}$ in dependence of the transferred power for different input voltages $V_{DC,1}$.

**TABLE 7.** Optimum Constant Operating Parameters

| Operating Parameter | Value |
|---|---|
| $V_{DC,1}$ | 700 V |
| $f_{S,DAB}$ | 140 kHz |
| $f_{S,AFE}$ | 40 kHz |

with higher switching frequencies, the optimum switching frequency $f_{S,DAB}$ decreases with higher transfer powers.

## VIII. SYSTEM OPTIMIZATION

With the described models for the two stages of the power supply, system optima can be found. The optimum parameters can either be found as constant parameters for the complete operation space or as dynamic operating parameters that depend on input and output conditions.

### A. OPTIMUM CONSTANT OPERATING PARAMETERS

First, the model is used to find the optimum constant operating parameters. The conventional approach is to minimize the maximum cooling effort and thus minimize the losses at maximum power. The DC-link voltage $V_{DC,1}$ must be chosen for the maximum input voltage which is $V_{AC,ll} = 480$ V. Accordingly, $V_{DC,1}$ is chosen to be 700 V. Highest losses occur at the minimum input voltage (comp. Ch. VI). For the constant operating parameters thus the optimum parameters for an input voltage of $V_{AC,ll} = 208$ V, a DC-link voltage of $V_{DC,1} = 700$ V and an output power of $P_{out} = 6$ kW are chosen.

The resulting optimum constant operating parameters are found with a brute-force optimization and given in Table 7.

### B. OPERATION SPACE OPTIMIZATION

In a second approach, the model is used to find optimum operating parameters for each set of input/output parameters.

Fig. 26 shows the optimization results for fixed input and output voltages ($V_{AC,ll} = 400$ V, $V_{out} = 600$ V) and a power transfer 1 kW $\leq P_{out} \leq$ 6 kW. The optimized parameters are the DC-link voltage ($400\text{ V} \cdot \sqrt{2} \leq V_{DC,1} \leq 480\text{ V} \cdot \sqrt{2}$), the

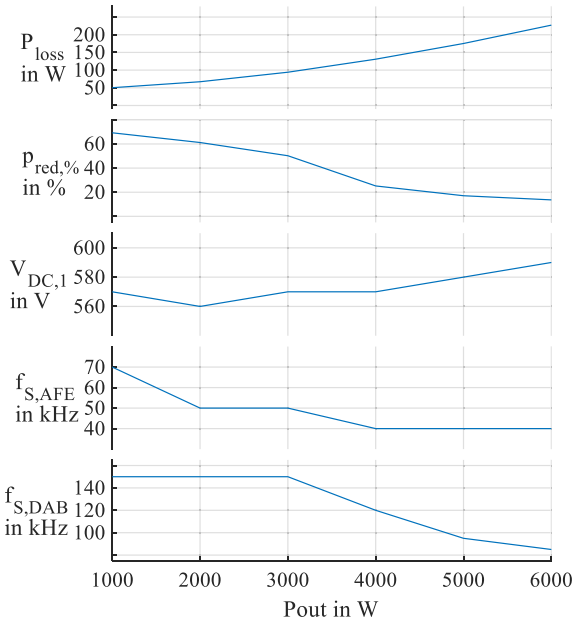


**FIGURE 26.** System power loss $P_{loss}$ and relative loss reduction $p_{red,\%}$ of the two stage power supply at $V_{AC,ll} = 400$ V and $V_{out} = 600$ V for a variable DC-link voltage $V_{DC,1}$ and variable switching frequencies of the DAB ($f_{S,DAB}$) and AFE ($f_{S,AFE}$).

AFE switching frequency (40 kHz $\leq f_{S,AFE} \leq$ 100 kHz) and the DAB switching frequency (85 kHz $\leq f_{S,DAB} \leq$ 150 kHz).

The relative loss reduction $p_{l,red,\%}$ is referred to the losses for constant parameters that are given in Table 7.

By using dynamic operating parameters losses at maximum power can be reduced by 14%. In turns, either cooling effort can be reduced, or output power increased. However, power supplies often run at partial load. At 50% output power ($P_{out} = 3$ kW) the model results promise a loss reduction of 48%. The main reason for the large reduction at lower losses is, that the optimization considers the soft switching region of the DAB and hence optimizes both switching frequency as well as DC-link voltage towards a soft switching operating point.

## IX. CONCLUSION AND OUTLOOK

The presented loss analysis and optimization model enable a detailed evaluation of system losses. Compared to previous work, the semiconductor loss model was optimized to work for high switching frequencies and the mixed transition included to account for higher ripple currents, which can occur when using WBG semiconductors. The magnetics loss model is based on analytical equations rather than numerical solvers. Overall, the model is optimized for calculation speed by using the spacing between fundamental and switching frequency and assuming constant losses for multiple adjacent switching instances.

Thus, the model allows to quickly analyse not only the total losses but also the loss distribution among power supply stages and down to the component level.

While previous work mainly focused on the optimization during the hardware design [8], [9], [10], [11], the presented optimization is especially useful for optimizing the operating parameters for a certain design at any operating condition. In this context, DC-link voltages as well as switching frequencies are seen as operating rather than design parameters. Consequently, they are optimized depending on the operating point. With the calculation efficient loss model, wide operation spaces can either be analysed during the control development or the model can even be implemented inside a microcontroller and optimization conducted during runtime.

By means of optimizing the operating parameters, the losses can be reduced by approximately 14% at full load and even 48% at half load operation. This loss reduction does not only reduce energy consumption but also leads to lower thermal component stress at partial load and thus higher lifetime expectancy. Also, the loss reduction may be used to expand the operation space that was analyzed in Ch. VI.

Future work should focus on in depth optimization that not only considers system losses but takes into account the loss distribution among the components. It should further extend the loss model for different converter topologies to enable loss reduction and smart derating concepts in yet more applications.

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